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A Case Study on Multi-Softcore Aided Hardware Architectures for Powerline MAC-Layer

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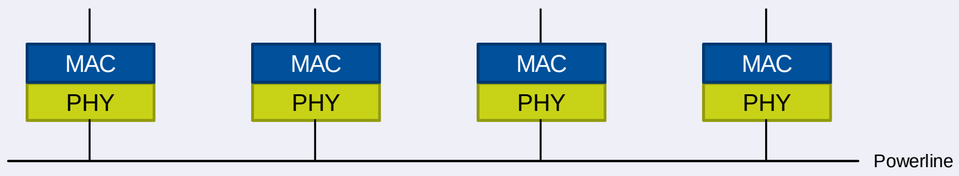
Motivation

- Powerline communication is a promising technology for connecting IoT applications
- Only power supply lines needed
- IoT requirements: cheap, low power dissipation

→ Resource-efficient MAC-Layer implementation needed



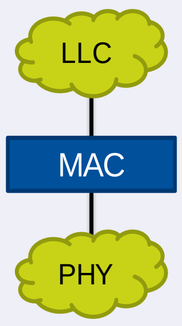
***Structure of a Powerline system**. Each station consists of a Media Access (**MAC**) and physical (**PHY**) layer. All stations are connected to a shared powerline.*

HomePlug MAC Layer

- Complex control flow (header generation/parsing) and number crunching (encryption, checksum calculation)
- Communication with LLC:
  - Complex control flow
  - No strict timing requirements
- Communication with PHY:
  - Simple control flow
  - Real-time requirements

Conflicting requirements

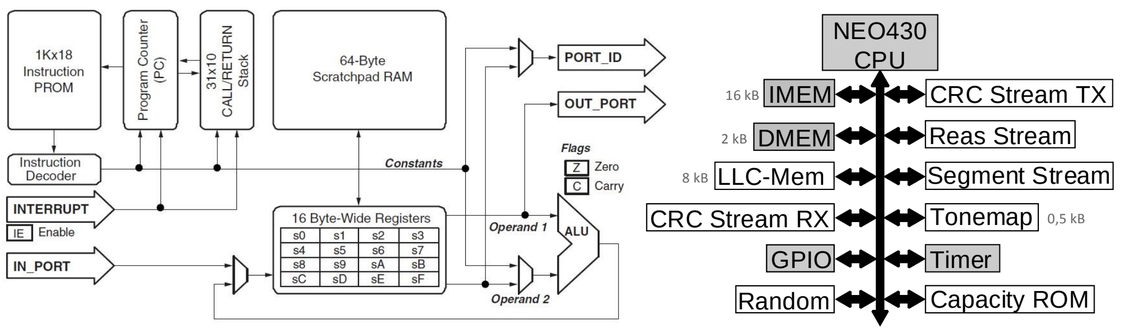
→ Special hardware architecture is required



*The **HomePlug protocol stack**. The MAC layer is controlled by the Link level connection (LLC) layer.*

Softcores

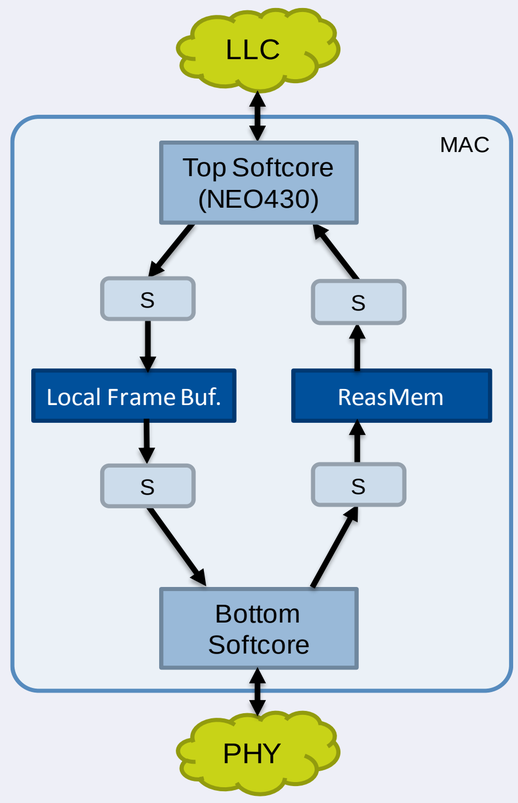
- **NEO430**
  - ISA compatible clone of the Texas Instruments MSP430
  - 16-bit architecture
  - high extensibility via system bus
  - low resource requirements (~650 LUT6)
- **PauloBlaze**
  - ISA compatible clone of the PicoBlaze
  - 8-bit architecture
  - very limited instruction set
  - very low resource requirement (~360 LUT6)



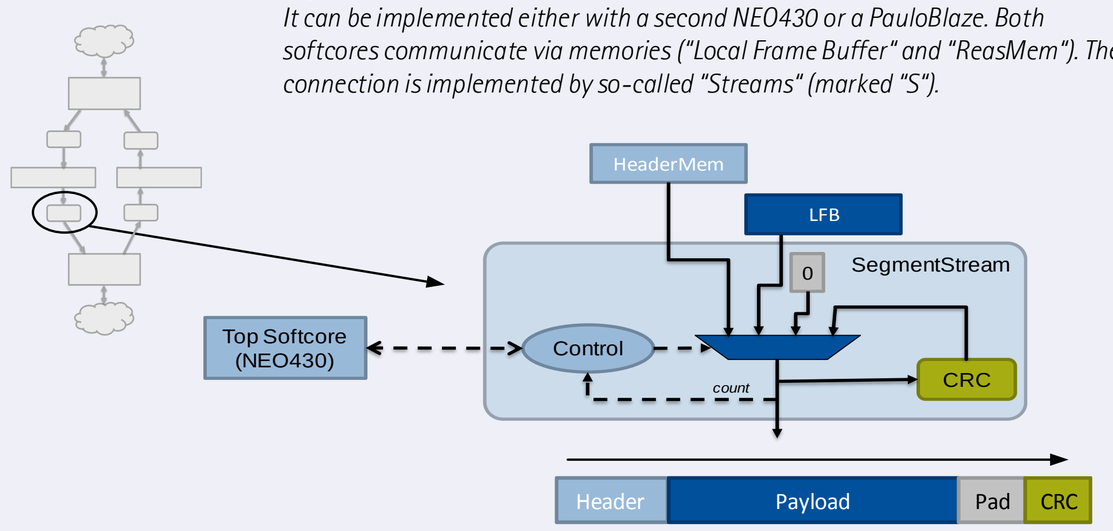
*Left: The **PauloBlaze** architecture. Right: The **NEO430** structure. White modules are custom designs.*

System architecture

- Heterogeneous Multi-Softcore architecture:
  - Top Softcore for LLC Interface (NEO430)
  - Bottom Softcore for PHY interface (NEO *or* PauloBlaze)
- Connected by shared memory
- Interfaces to memory are „Pseudo-FIFO interface“
  - Perform computations/ multiplexing on-the-fly
  - Allow to maintain very high throughput despite the slow softcores



***System architecture overview**. The **Top Softcore** is connected to the LLC layer. It is implemented with a NEO430. The **Bottom Softore** is connected to the PHY layer. It can be implemented either with a second NEO430 or a PauloBlaze. Both softcores communicate via memories (“Local Frame Buffer“ and “ReasMem“). The connection is implemented by so-called “Streams“ (marked “S“).*



*Implementation of the **Segment Stream**, connecting the buffer for outgoing packages (LFB) with the PHY layer. At the start of the package, bytes from the **header memory** are read. After reading 17 bytes (the size of the header), the control unit switches the multiplexer to the LFB and **payload bytes** are read. After a configurable amount of payload, **padding** is inserted. During the whole transmission, the **CRC checksum** of all transferred data is calculated. It will be automatically appended after the padding.*
For the PYH layer the stream is a simple FIFO from which it can read linearly at any desired speed.

Evaluation

- Three variants were implemeted:

Variant	LUTs	Register	DSPs	BlockRAM	Freq. (MHz)
w/o Softcores	7845	5718	1	21	160
2xNEO430	1941 (-75 %)	1401 (-75 %)	0	10,5 (-50 %)	130 (-19 %)
1xNEO+1xPauloBlaze	1730 (-78 %)	1198 (-79 %)	0	9,5 (-55 %)	104 (-35 %)

- Using Softcores makes the design **smaller**, **easier to maintain** and **more flexible**
- The PauloBlaze version is even smaller, but requires assembler programming

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References

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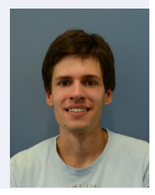
[2] N. Rother, Konzeptionierung und Implementierung einer hybriden MAC-Layer-Architektur für Paket-basierte Powerline Kommunikation auf einem FPGA, *Master thesis, Leibniz Universität Hannover*



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