Developing a novel method of alignment to buried cavities in C-SOI wafers

Christopher Mountain[1], Marta Kluba[2], Ronald Dekker[3]

[1] Dept. of Bioengineering, The University of Sheffield, England, cmountain1@sheffield.ac.uk; [2] Dept. of Microelectronics, TU/Delft, The Netherlands, M.M.Kluba@tudelft.nl; [3] Dept. of Microelectronics, TU/Delft, The Netherlands; R.Dekker@tudelft.nl

Introduction

Cavity-SOI wafers are an emerging form of 'smart' substrate used in MEMS processing, which feature cavities inside the silicon that are used to enhance manufacturing [1] or can be integrated into the functional device structure itself [2].

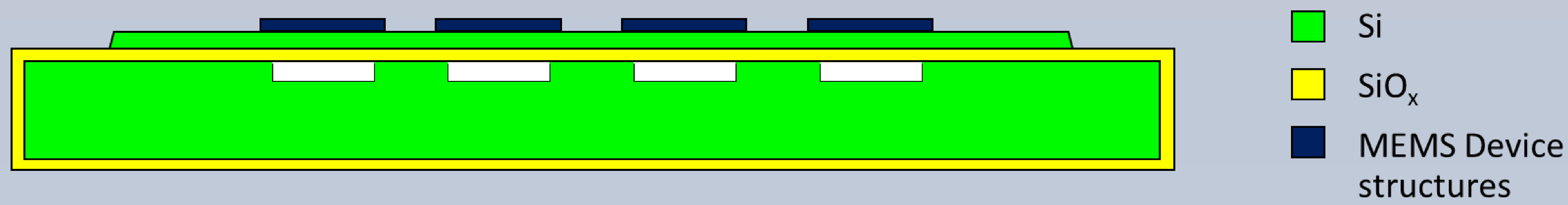

Figure 1. Example cross-section of a C-SOI wafer showing pre-fabricated cavities inside the handle wafer, used for CMUT production

Device fabrication subsequently relies on accurate alignment of top-layer structures to the cavities below. Existing methods are costly, require specialized equipment [3, 4] or interfere with the wafer bonding process.

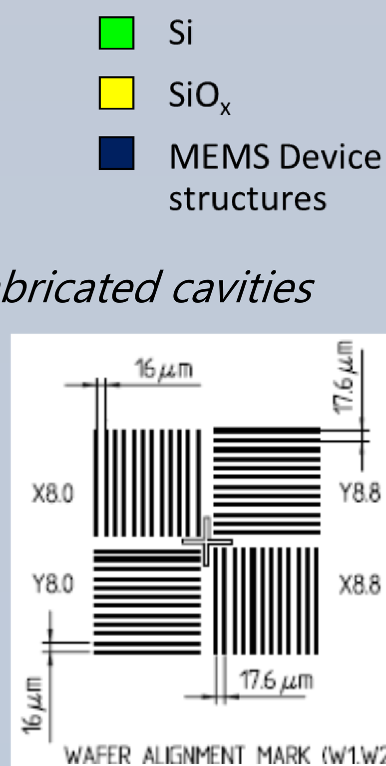

Figure 2. Schematic of a standard ASML alignment marker used for wafer alignment during photolithography [5]

Aims

Develop a process for patterning alignment markers on the handle wafer, which are detectable through the top device layer.

Investigate:

1. A feasible alignment strategy, with two possible options:
   a) Viewing markers through the device-layer silicon
   b) Non-standard positioning of markers
2. Problems caused by using markers out of the surface plane

Method

1. a) Optical physics was used to mathematically model the interactions between the stepper laser alignment system and the markers on the handle wafer.

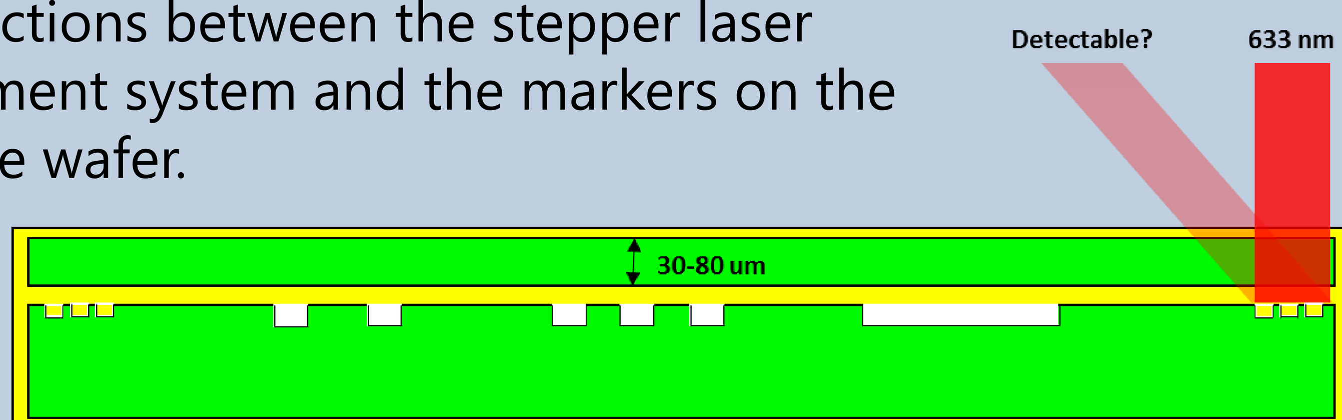

Figure 3. Cross-section of a C-SOI wafer with alignment markers etched alongside the cavities, such that the alignment laser views them through the silicon device layer.

1. b) Alignment markers were fabricated within 2-4 mm of the wafer edge, where the top silicon can be removed. It was assessed whether this hinders manufacturability or detectability.

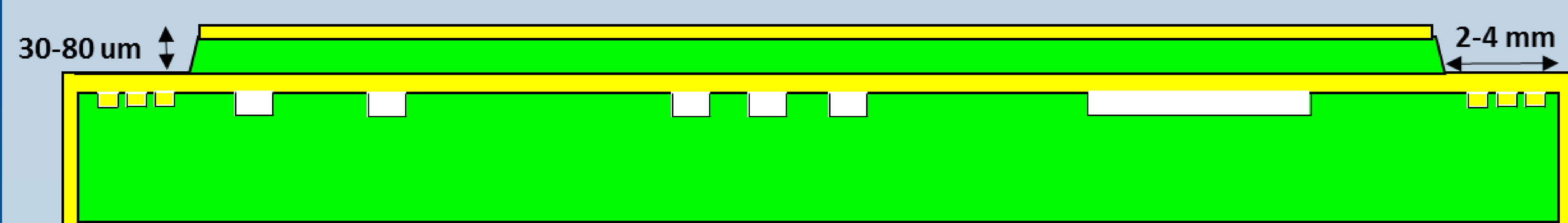

Figure 4. Alignment markers placed in a non-standard position, close enough to the wafer edge that 'terracing' reveals them for optical detection.

2. Prototypes simulating the geometry of C-SOI wafers were produced. The device layer was patterned with new markers to characterize any error that was introduced.

Figure 5. Cross-section showing the layers fabricated to create a geometric simulation of the proposed 'terraced' wafer.

Results

1. a) Model results suggest that the laser power would be attenuated by at least two orders of magnitude with the addition of a 30 um silicon layer on top, making alignment infeasible.

1. b) Markers nearer to the wafer edge were over-etched by up to 10%. However, this had a negligible effect on the signal quality required for alignment.

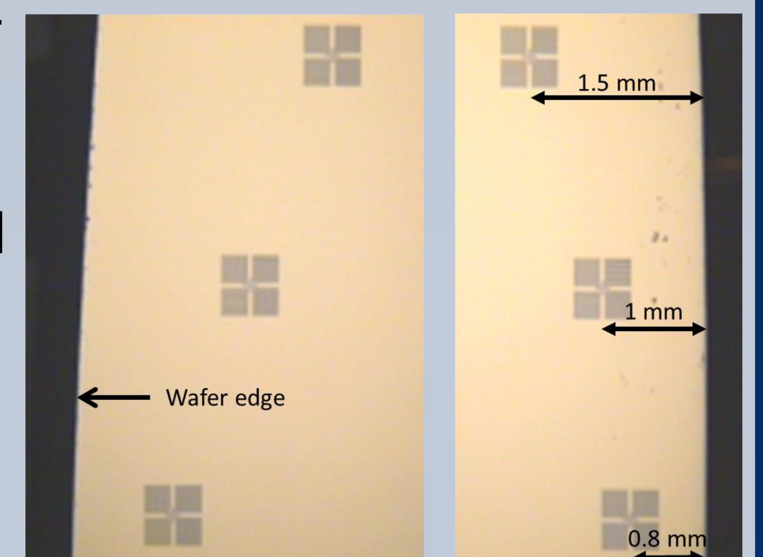

Figure 6. Microscopy showing a range of alignment markers etched as close as 0.8 mm to the wafer edge

2. The stepper was successfully able to align to markers up to 80 um below the surface plane of the wafer. At this depth, the maximum average offset in X and Y was 37 nm (SD = 41 nm).

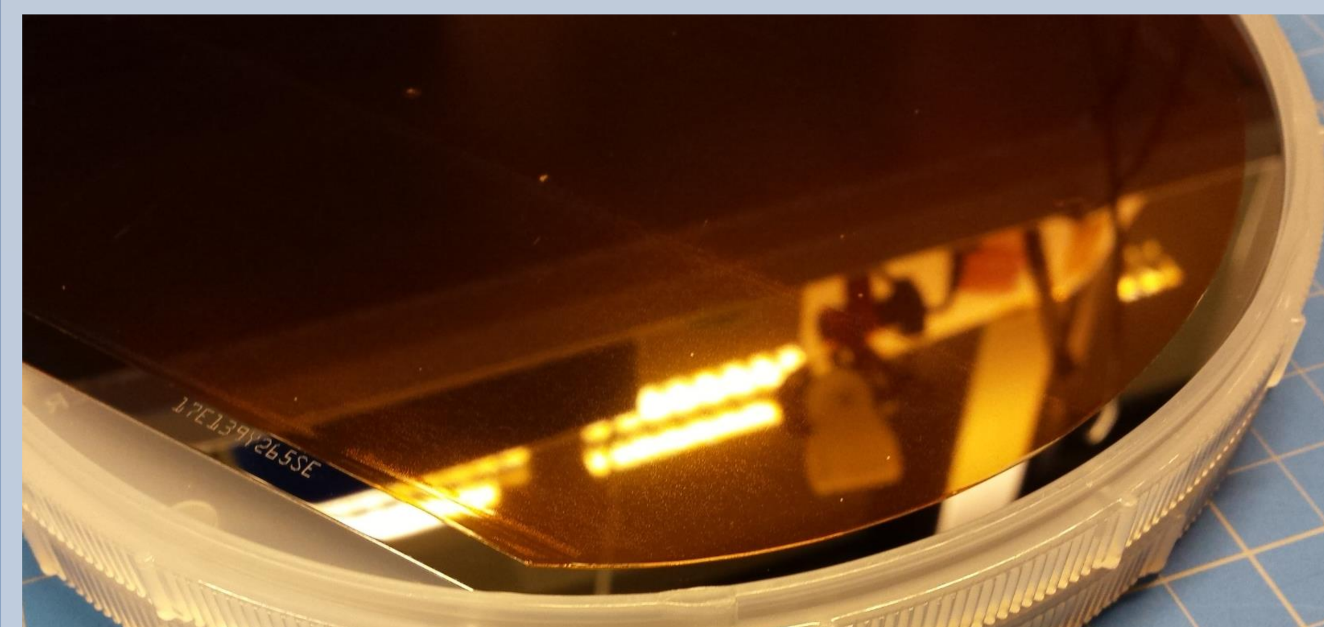

Figure 7. Photograph of a simulation C-SOI wafer, with 80 um thick polymer 'terrace'.

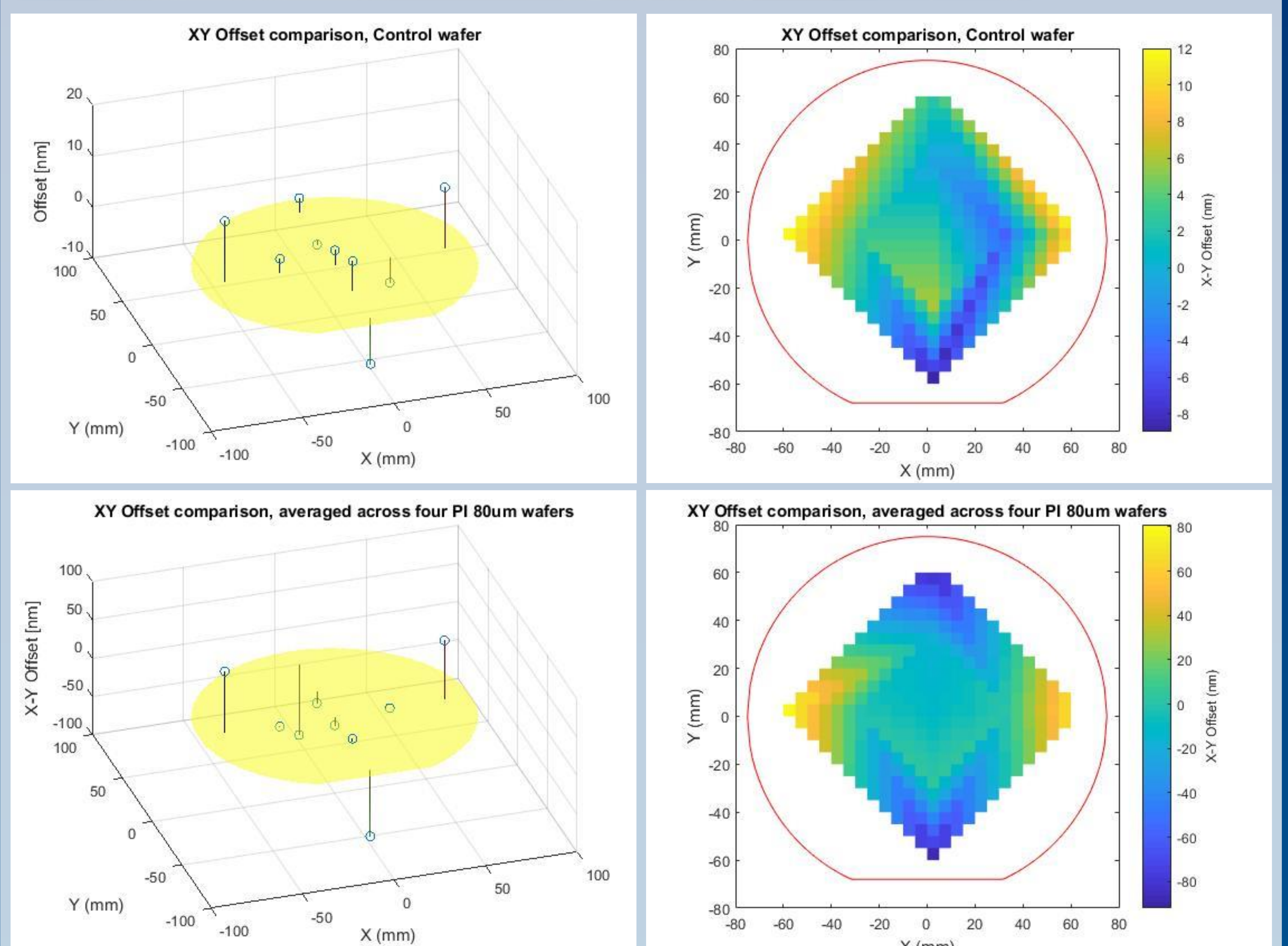

Figure 8. Comparison of error (offsets) in lithography at the wafer surface plane. The results suggest that error in X and Y increases as the magnitudes of X and Y approach maximum across the wafer.

Conclusion

The proposed process is feasible, since functional alignment markers can be fabricated on the handle wafer, introducing some manageable error to surface plane lithography.

References:

[1] Okmetic. (2018, 06/02/18). *SOI WAFERS*.
[2] A. S. ERGUN , G. G. YARALIOGLU, O. ORALKAN, and B. T. KHURI-YAKUB, C. T. Leondes, Ed. *MEMS/NEMS Handbook Techniques and Applications*. Springer, 2006.
[3] ASML. (2007, 06/02/18). *Recent developments in double sided alignment and back-side alignment*
[4] C. Wang and T. Suga, "Nanoprecision aligned wafer direct bonding and its outlook," ed, 2011, pp. 1-4.
[6] L. Fuller and S. Bolster. (2014, 06/02/08). *Lithography Using ASML Stepper*.

The University Of Sheffield. OKMETIC InForMed TU Delft Delft University of Technology PHILIPS